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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,765	08/28/2003	Teruhisa Obara	OKI 368	5864

23995 7590 12/27/2006	EXAMINER	
RABIN & Berdo, PC	SIDDIQUI, SAQIB JAVAID	
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WASHINGTON, DC 20005		

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/27/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

	Application No.	Applicant(s)
	10/649,765	OBARA, TERUHISA
Office Action Summary	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>22 November 2006</u>.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-14</u> is/are pending in the application.

   4a) Of the above claim(s) <u>13-14</u> is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-12</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All b)☐ Some * c)☐ None of:

   1.☐ Certified copies of the priority documents have been received.

   2.☐ Certified copies of the priority documents have been received in Application No. _____.

   3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Applicant's response was received and entered November 22, 2006.

-        Claims 1-12 are pending. Claims 1, 4, 7 and 10 are amended.

-        Claims 13-14 are canceled.

-        Application is currently pending.

Response to Amendment

Applicant's arguments and amendments with respect to claims 1-12 filed

November 22, 2006 have been considered but they are not persuasive.

Applicant contends that Whetsel does not teach a parallel/serial converter

comprising a selector circuit and a flip-flop. Examiner respectfully disagrees.

Whetsel states "the scan collector circuit is basically a parallel-input serial-output

shift register." Whetsel does not describe the structure of a parallel-input serial-output

shift register, however prior arts of record show that a selection circuit and a flip-flop are

considered basic elements of a parallel-input serial-output shift registers. Therefore,

since Whetsel teaches a parallel-input serial-output shift register, it incorporates a

selection circuit and a flip-flop within the shift register. Evidence for Examiner's

contention can be found in US Pat no. (4,499,454, 5,012,240, 5,119,379, 5,247,652 and

5,926,120). Further, Philips data sheet for a 8-bit parallel-input serial-output shift register

(Figure 5), also provides support for Examiner's contentions.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Whetsel US Pat no. 6,242,269 B1, and further in view of Eriksson et al. US Patent no.

6,169,500 B1

As per claim 1:

Whetsel substantially teaches a semiconductor integrated circuit (Figure 8 # 700)

comprising: m scan chains (wherein m is an integer greater than 1) each of which

includes a plurality of logic circuits and a plurality of scan registers connected alternately

in series (Figure 8 # 924), each of the scan chains including a first logic circuit having a

data input terminal (Figure 8 # 800, column 7, lines 53-56), a first scan register connected

to the first logic circuit (Figure 8 # 800, column 7, lines 53-56), the first scan register

having a test input terminal (Figure 8 # 900, column 8, lines 6-8), and a last scan register

having an output terminal (Figure 8 # 844, column 7, lines 58-61); a serial/parallel

conversion circuit connected to the test input terminals of the first scan registers of the

scan chains (column 1, lines 65-66), and a parallel/serial conversion circuit connected to

the output terminals of the last scan registers of the scan chains (column 1, lines 66-67),

wherein the parallel/serial conversion circuit comprises a selector and a flip-flop (Figure

10 # 1026).

Whetsel does not explicitly teach a semiconductor integrated circuit wherein; the

scan registers are being operated in response to a clock signal and the conversion

circuits converting data in response to a multiplied clock signal having a frequency being

m times of that of the clock signal.

However, Eriksson et al. in an analogous art, teaches a semiconductor integrated

circuit wherein; the scan registers are being operated in response to a clock signal

(Figure 2 "CLK", column 2, lines 54-56), the serial/parallel conversion circuit (Fig 6 # 50

a-c) converting serial data into parallel data in response to a multiplied clock signal

having a frequency being m times of that of the clock signal (Figure 6, "CLK184a-c"); and

the parallel/serial conversion circuit (Fig 6 # 60) converting parallel data received from the

scan chains into serial data in response to the multiplied clock signal (Fig 6, "CLK184d").

Therefore it would have been obvious to one of ordinary skill in the art at the time the

invention was made to use clock signal within to control the operations of the scan chains

and conversion circuits in the teaching of Whetsel. This modification would have been

obvious to one of ordinary skill in the art because one of ordinary skill in the art would

have recognized that using a clock signal to control the operation of a scan chain is a

commonplace practice in the art and delaying the incoming signals in relation to the clock

signals will reduce the risk of errors (Eriksson et al., column 1, lines 53-56).

As per claim 2:

Whetsel substantially teaches a semiconductor integrated circuit (Figure 8 # 700)

comprising: m scan chains (wherein m is an integer greater than 1) each of which

includes a plurality of logic circuits and a plurality of scan registers connected alternately

in series (Figure 8 # 924), each of the scan chains including a first logic circuit having a

data input terminal (Figure 8 # 800, column 7, lines 53-56), a first scan register connected

to the first logic circuit (Figure 8 # 800, column 7, lines 53-56), the first scan register

having a test input terminal (Figure 8 # 900, column 8, lines 6-8), and a last scan register

having an output terminal (Figure 8 # 844, column 7, lines 58-61); a serial/parallel

conversion circuit connected to the test input terminals of the first scan registers of the

scan chains (column 1, lines 65-66), and a parallel/serial conversion circuit connected to

the output terminals of the last scan registers of the scan chains (column 1, lines 66-67),

further comprising a multiplication circuit connected to the serial/parallel conversion

circuit and the parallel/serial conversion circuit (column 2, lines 3-13).

Whetsel does not explicitly teach a semiconductor integrated circuit wherein; the

scan registers are being operated in response to a clock signal, the conversion circuits

converting data in response to a multiplied clock signal having a frequency being m times

of that of the clock signal, and the multiplication circuit generating the multiplied clock

signal based on the clock signal received thereto.

However, Eriksson et al. in an analogous art, teaches a semiconductor integrated circuit wherein; the scan registers are being operated in response to a clock signal (Figure 2 "CLK", column 2, lines 54-56), the serial/parallel conversion circuit (Fig 6 # 50 a-c) converting serial data into parallel data in response to a multiplied clock signal having a frequency being m times of that of the clock signal (Figure 6, "CLK184a-c"); the parallel/serial conversion circuit (Fig 6 # 60) converting parallel data received from the scan chains into serial data in response to the multiplied clock signal (Fig 6, "CLK184d"), and further comprising a multiplication circuit connected to the serial/parallel conversion circuit and the parallel/serial conversion circuit (column 1, lines 31-33), the multiplication circuit generating the multiplied clock signal based on the clock signal received thereto (column 2 lines 54-60). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use clock signal within to control the operations of the scan chains and conversion circuits in the teaching of Whetsel. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that using a clock signal to control the operation of a scan chain is a commonplace practice in the art and delaying the incoming signals in relation to the clock signals will reduce the risk of errors (Eriksson et al., column 1, lines 53-56).

As per claims 3-5:

Whetsel substantially teaches a semiconductor integrated circuit (Figure 8 # 700) comprising: m scan chains (wherein m is an integer greater than 1) each of which includes a plurality of logic circuits and a plurality of scan registers connected alternately

in series (Figure 8 # 924), each of the scan chains including a first logic circuit having a

data input terminal (Figure 8 # 800, column 7, lines 53-56), a first scan register

connected to the first logic circuit (Figure 8 # 800, column 7, lines 53-56), the first scan

register having a test input terminal (Figure 8 # 900, column 8, lines 6-8), a last scan

register having an output terminal (Figure 8 # 844, column 7, lines 58-61); a

serial/parallel conversion circuit connected to the test input terminals of the first scan

registers of the scan chains (column 1, lines 65-66), and a parallel/serial conversion

circuit connected to the output terminals of the last scan registers of the scan chains

(column 1, lines 66-67), further comprising a multiplication circuit connected to the

serial/parallel conversion circuit and the parallel/serial conversion circuit (column 2, lines

3-13), wherein the serial/parallel conversion circuit including a plurality of flip-flops

connected in series (column 4, lines 54-61), and a plurality of selectors (Figure 8 # 876,

column 7, lines 64-67), wherein each of the serial registers includes a selector and a flip-

flop.

Whetsel does not explicitly teach a semiconductor integrated circuit wherein; the

scan registers are being operated in response to a clock signal, the conversion circuits

converting data in response to a multiplied clock signal having a frequency being m

times of that of the clock signal, and wherein each of the serial registers includes a

selector and a flip-flop being operated in response to the clock signal.

However, Eriksson et al. in an analogous art, teaches a semiconductor integrated

circuit wherein; the scan registers are being operated in response to a clock signal

(Figure 2 "CLK", column 2, lines 54-56), the serial/parallel conversion circuit (Fig 6 # 50

a-c) converting serial data into parallel data in response to a multiplied clock signal

having a frequency being m times of that of the clock signal (Figure 6, "CLK184a-c"); the

parallel/serial conversion circuit (Fig 6 # 60) converting parallel data received from the

scan chains into serial data in response to the multiplied clock signal (Fig 6, "CLK184d"),

and wherein each of the serial registers includes a selector and a flip-flop being

operated in response to the clock signal (Figure 6 #71 a-f, "CLK184a-d") . Therefore it

would have been obvious to one of ordinary skill in the art at the time the invention was

made to use clock signal within to control the operations of the scan chains and

conversion circuits in the teaching of Whetsel. This modification would have been

obvious to one of ordinary skill in the art because one of ordinary skill in the art would

have recognized that using a clock signal to control the operation of a scan chain is a

commonplace practice in the art and delaying the incoming signals in relation to the

clock signals will reduce the risk of errors (Eriksson et al., column 1, lines 53-56).

As per claim 6:

Whetsel substantially teaches a semiconductor integrated circuit (Figure 8 # 700)

comprising: m scan chains (wherein m is an integer greater than 1) each of which

includes a plurality of logic circuits and a plurality of scan registers connected alternately

in series (Figure 8 # 924), each of the scan chains including a first logic circuit having a

data input terminal (Figure 8 # 800, column 7, lines 53-56), a first scan register connected

to the first logic circuit (Figure 8 # 800, column 7, lines 53-56), the first scan register

having a test input terminal (Figure 8 # 900, column 8, lines 6-8), and a last scan register

having an output terminal (Figure 8 # 844, column 7, lines 58-61); a serial/parallel

conversion circuit connected to the test input terminals of the first scan registers of the

scan chains (column 1, lines 65-66), and a parallel/serial conversion circuit connected to

the output terminals of the last scan registers of the scan chains (column 1, lines 66-67),

wherein the output terminal of the last scan register of one of the scan chains (Figure 8 #

946) is connected to the data input terminal of the first logic circuit of another one of the

scan chains (Figure 8, # 964 and "PSC").

Whetsel does not explicitly teach a semiconductor integrated circuit wherein; the

scan registers are being operated in response to a clock signal and the conversion

circuits converting data in response to a multiplied clock signal having a frequency being

m·times of that of the clock signal.

However, Eriksson et al. in an analogous art, teaches a semiconductor integrated

circuit wherein; the scan registers are being operated in response to a clock signal

(Figure 2 "CLK", column 2, lines 54-56), the serial/parallel conversion circuit (Fig 6 # 50

a-c) converting serial data into parallel data in response to a multiplied clock signal

having a frequency being m times of that of the clock signal (Figure 6, "CLK184a-c"); and

the parallel/serial conversion circuit (Fig 6 # 60) converting parallel data received from the

scan chains into serial data in response to the multiplied clock signal (Fig 6, "CLK184d").

Therefore it would have been obvious to one of ordinary skill in the art at the time the

invention was made to use clock signal within to control the operations of the scan chains

and conversion circuits in the teaching of Whetsel. This modification would have been

obvious to one of ordinary skill in the art because one of ordinary skill in the art would

have recognized that using a clock signal to control the operation of a scan chain is a

commonplace practice in the art and delaying the incoming signals in relation to the clock signals will reduce the risk of errors (Eriksson et al., column 1, lines 53-56).

As per claim 7:

Whetsel substantially teaches a semiconductor integrated circuit (Figure 8 # 700) comprising a plurality of scan chains each of which includes a first logic circuit having a data input terminal (Figure 8 # 800, column 7, lines 53-56), a first scan register connected to the first logic circuit (Figure 8 # 800, column 7, lines 53-56), the first scan register having a test input terminal (Figure 8 # 900, column 8, lines 6-8), and a last scan register having an output terminal (Figure 8 # 844, column 7, lines 58-61); a serial/parallel conversion circuit connected to the test input terminals of the first scan registers of the scan chains (column 1, lines 65-66), and a parallel/serial conversion circuit connected to the output terminals of the last scan registers of the scan chains (column 1, lines 66-67), wherein the parallel/serial conversion circuit comprises a selector and a flip-flop (Figure 10 # 1026).

Whetsel does not explicitly teach a semiconductor integrated circuit wherein; the scan registers are being operated in response to a clock signal and the conversion circuits converting data in response to a multiplied clock signal having a frequency being m times of that of the clock signal.

However, Eriksson et al. in an analogous art, teaches a semiconductor integrated circuit wherein; the scan registers are being operated in response to a clock signal (Figure 2 "CLK", column 2, lines 54-56), the serial/parallel conversion circuit (Fig 6 # 50 a-c) converting serial data into parallel data in response to a multiplied clock signal

having a frequency being m times of that of the clock signal (Figure 6, "CLK184a-c"); and

the parallel/serial conversion circuit (Fig 6 # 60) converting parallel data received from the

scan chains into serial data in response to the multiplied clock signal (Fig 6, "CLK184d").

Therefore it would have been obvious to one of ordinary skill in the art at the time the

invention was made to use clock signal within to control the operations of the scan chains

and conversion circuits in the teaching of Whetsel. This modification would have been

obvious to one of ordinary skill in the art because one of ordinary skill in the art would

have recognized that using a clock signal to control the operation of a scan chain is a

commonplace practice in the art and delaying the incoming signals in relation to the clock

signals will reduce the risk of errors (Eriksson et al., column 1, lines 53-56).

As per claim 8:

Whetsel teaches a semiconductor integrated circuit (Figure 8 # 700) comprising a

plurality of scan chains each of which includes a first logic circuit having a data input

terminal (Figure 8 # 800, column 7, lines 53-56), a first scan register connected to the first

logic circuit (Figure 8 # 800, column 7, lines 53-56), the first scan register having a test

input terminal (Figure 8 # 900, column 8, lines 6-8), and a last scan register having an

output terminal (Figure 8 # 844, column 7, lines 58-61); a serial/parallel conversion

circuit connected to the test input terminals of the first scan registers of the scan chains

(column 1, lines 65-66), and a parallel/serial conversion circuit connected to the output

terminals of the last scan registers of the scan chains (column 1, lines 66-67), further

comprising a multiplication circuit connected to the serial/parallel conversion circuit and

the parallel/serial conversion circuit (column 2, lines 3-13).

Whetsel does not explicitly teach a semiconductor integrated circuit wherein; the scan registers are being operated in response to a clock signal, the conversion circuits converting data in response to a multiplied clock signal having a frequency being m times of that of the clock signal, and the multiplication circuit generating the multiplied clock signal based on the clock signal received thereto.

However, Eriksson et al. in an analogous art, teaches a semiconductor integrated circuit wherein; the scan registers are being operated in response to a clock signal (Figure 2 "CLK", column 2, lines 54-56), the serial/parallel conversion circuit (Fig 6 # 50 a-c) converting serial data into parallel data in response to a multiplied clock signal having a frequency being m times of that of the clock signal (Figure 6, "CLK184a-c"); the parallel/serial conversion circuit (Fig 6 # 60) converting parallel data received from the scan chains into serial data in response to the multiplied clock signal (Fig 6, "CLK184d"), and further comprising a multiplication circuit connected to the serial/parallel conversion circuit and the parallel/serial conversion circuit (column 1, lines 31-33), the multiplication circuit generating the multiplied clock signal based on the clock signal received thereto (column 2 lines 54-60). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use clock signal within to control the operations of the scan chains and conversion circuits in the teaching of Whetsel. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that using a clock signal to control the operation of a scan chain is a commonplace practice in the art and delaying the incoming

signals in relation to the clock signals will reduce the risk of errors (Eriksson et al.,

column 1, lines 53-56).

As per claims 9-11:

Whetsel substantially teaches a semiconductor integrated circuit (Figure 8 # 700)

comprising a plurality of scan chains each of which includes a first logic circuit having a

data input terminal (Figure 8 # 800, column 7, lines 53-56), a first scan register

connected to the first logic circuit (Figure 8 # 800, column 7, lines 53-56), the first scan

register having a test input terminal (Figure 8 # 900, column 8, lines 6-8), a last scan

register having an output terminal (Figure 8 # 844, column 7, lines 58-61); a

serial/parallel conversion circuit connected to the test input terminals of the first scan

registers of the scan chains (column 1, lines 65-66), and a parallel/serial conversion

circuit connected to the output terminals of the last scan registers of the scan chains

(column 1, lines 66-67), further comprising a multiplication circuit connected to the

serial/parallel conversion circuit and the parallel/serial conversion circuit (column 2, lines

3-13), wherein the serial/parallel conversion circuit including a plurality of flip-flops

connected in series (column 4, lines 54-61), and a plurality of selectors (Figure 8 # 876,

column 7, lines 64-67), wherein each of the serial registers includes a selector and a flip-

flop.

Whetsel does not explicitly teach a semiconductor integrated circuit wherein; the

scan registers are being operated in response to a clock signal, the conversion circuits

converting data in response to a multiplied clock signal having a frequency being m

times of that of the clock signal, and wherein each of the serial registers includes a selector and a flip-flop being operated in response to the clock signal.

However, Eriksson et al. in an analogous art, teaches a semiconductor integrated circuit wherein; the scan registers are being operated in response to a clock signal (Figure 2 "CLK", column 2, lines 54-56), the serial/parallel conversion circuit (Fig 6 # 50 a-c) converting serial data into parallel data in response to a multiplied clock signal having a frequency being m times of that of the clock signal (Figure 6, "CLK184a-c"); the parallel/serial conversion circuit (Fig 6 # 60) converting parallel data received from the scan chains into serial data in response to the multiplied clock signal (Fig 6, "CLK184d"), and wherein each of the serial registers includes a selector and a flip-flop being operated in response to the clock signal (Figure 6 #71 a-f, "CLK184a-d") . Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use clock signal within to control the operations of the scan chains and conversion circuits in the teaching of Whetsel. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that using a clock signal to control the operation of a scan chain is a commonplace practice in the art and delaying the incoming signals in relation to the clock signals will reduce the risk of errors (Eriksson et al., column 1, lines 53-56).

As per claim 12:

Whetsel substantially teaches a semiconductor integrated circuit (Figure 8 # 700) comprising a plurality of scan chains each of which includes a first logic circuit having a data input terminal (Figure 8 # 800, column 7, lines 53-56), a first scan register connected

to the first logic circuit (Figure 8 # 800, column 7, lines 53-56), the first scan register

having a test input terminal (Figure 8 # 900, column 8, lines 6-8), and a last scan register

having an output terminal (Figure 8 # 844, column 7, lines 58-61); a serial/parallel

conversion circuit connected to the test input terminals of the first scan registers of the

scan chains (column 1, lines 65-66), and a parallel/serial conversion circuit connected to

the output terminals of the last scan registers of the scan chains (column 1, lines 66-67),

wherein the selectors of the serial registers are operated in response to a mode signal

(Figure 10 "MUX").

Whetsel does not explicitly teach a semiconductor integrated circuit wherein; the

scan registers are being operated in response to a clock signal and the conversion

circuits converting data in response to a multiplied clock signal having a frequency being

m times of that of the clock signal.

However, Eriksson et al. in an analogous art, teaches a semiconductor integrated

circuit wherein; the scan registers are being operated in response to a clock signal

(Figure 2 "CLK", column 2, lines 54-56), the serial/parallel conversion circuit (Fig 6 # 50

a-c) converting serial data into parallel data in response to a multiplied clock signal

having a frequency being m times of that of the clock signal (Figure 6, "CLK184a-c"); and

the parallel/serial conversion circuit (Fig 6 # 60) converting parallel data received from the

scan chains into serial data in response to the multiplied clock signal (Fig 6, "CLK184d").

Therefore it would have been obvious to one of ordinary skill in the art at the time the

invention was made to use clock signal within to control the operations of the scan chains

and conversion circuits in the teaching of Whetsel. This modification would have been

obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that using a clock signal to control the operation of a scan chain is a commonplace practice in the art and delaying the incoming signals in relation to the clock signals will reduce the risk of errors (Eriksson et al., column 1, lines 53-56).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Saqib Siddiqui
Art Unit 2138
11/07/2006

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SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100